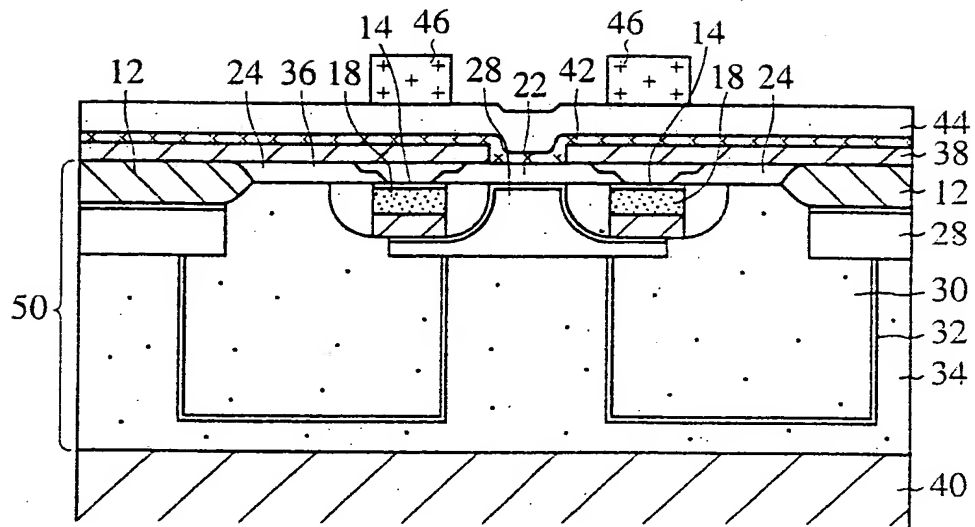


FIG.1



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FIG.2A

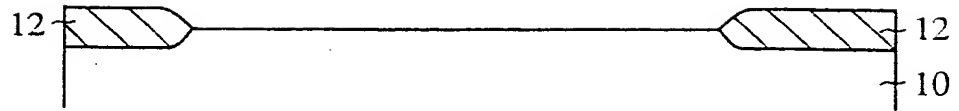


FIG.2B

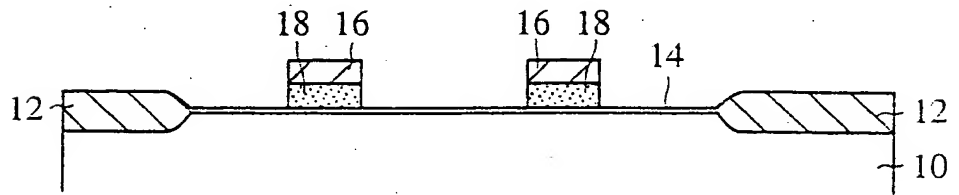


FIG.2C

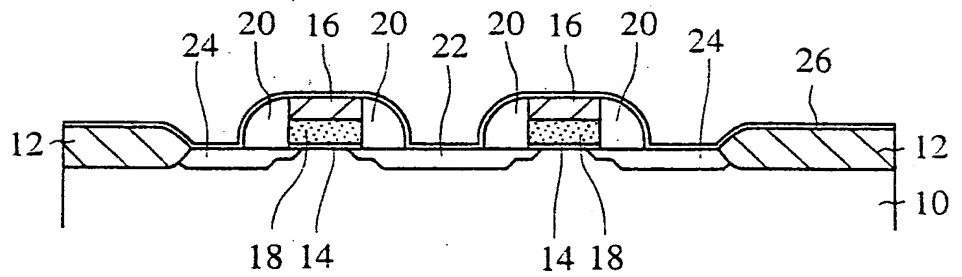
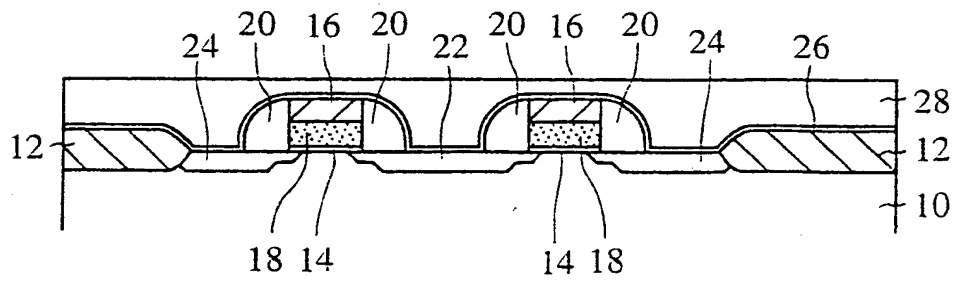


FIG.2D



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FIG.3A

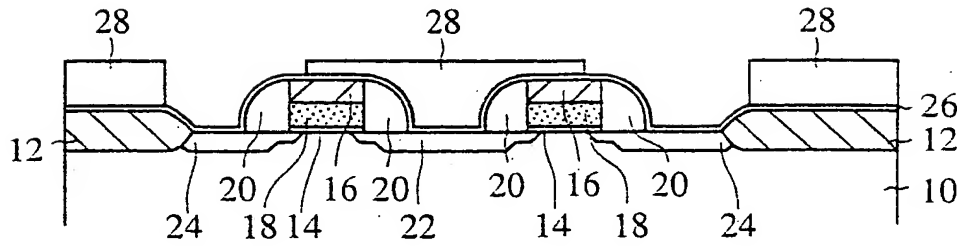


FIG.3B

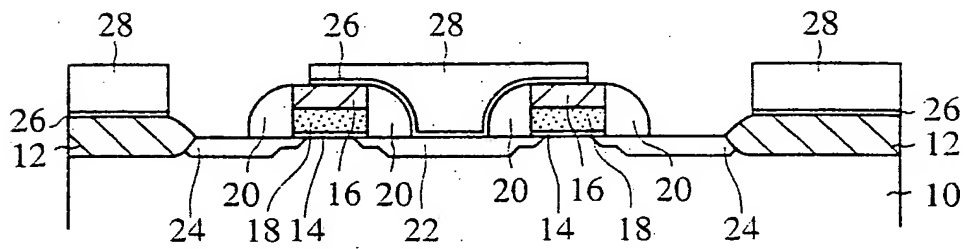


FIG.3C

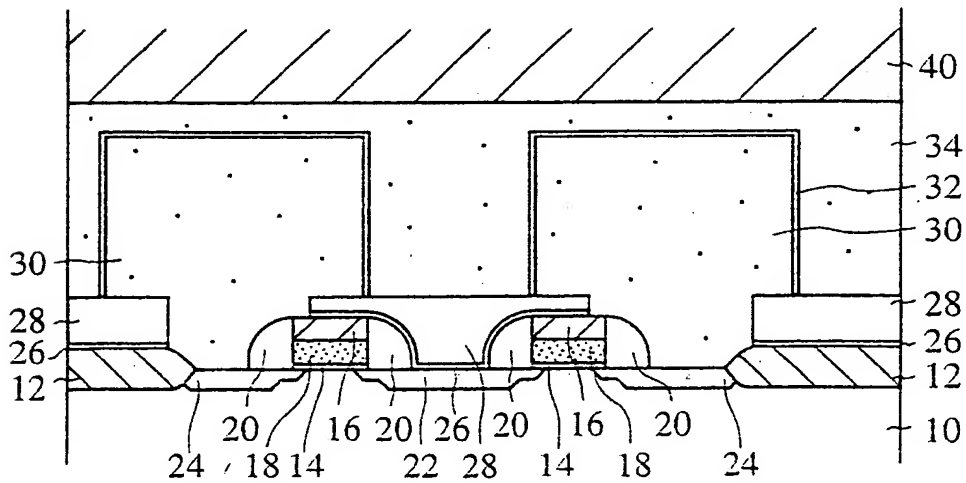


FIG.4A

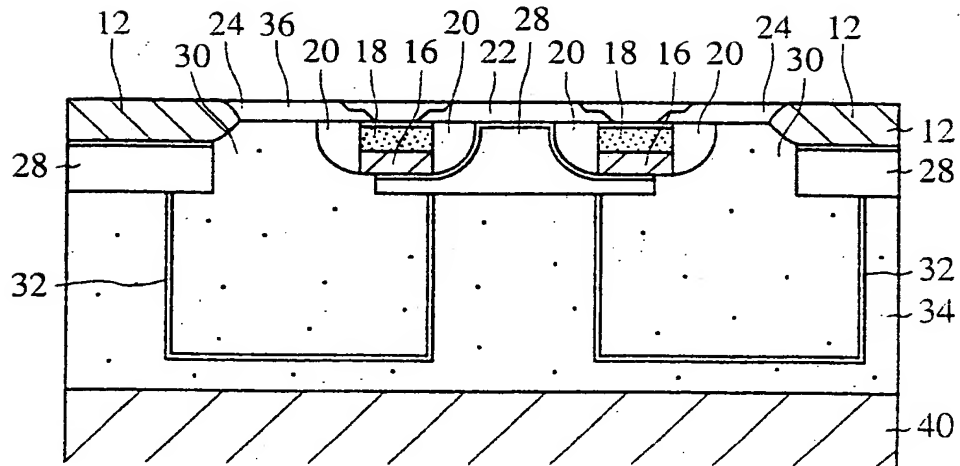


FIG.4B

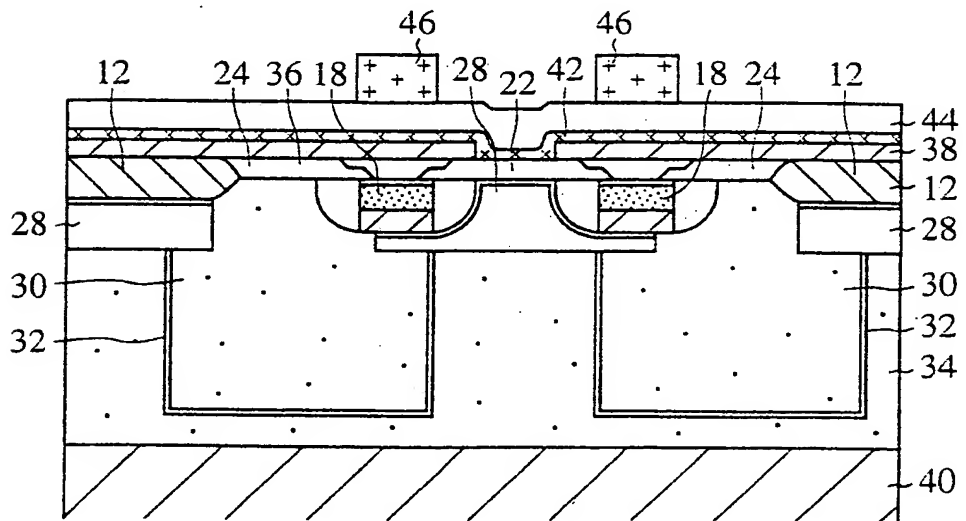


FIG. 4A

FIG.5A

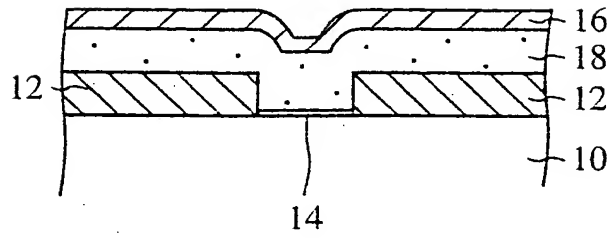


FIG.5B

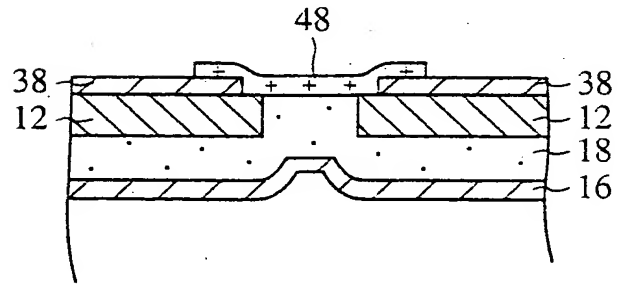
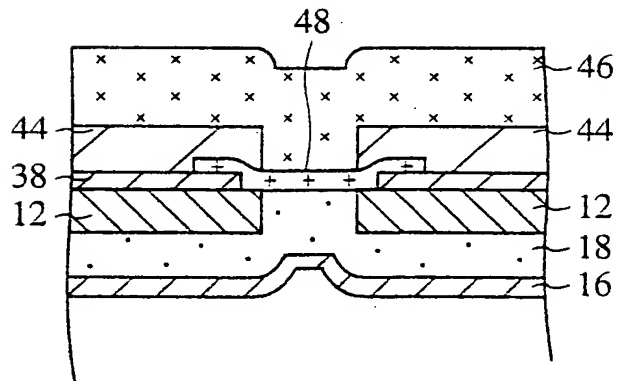


FIG.5C



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FIG.6

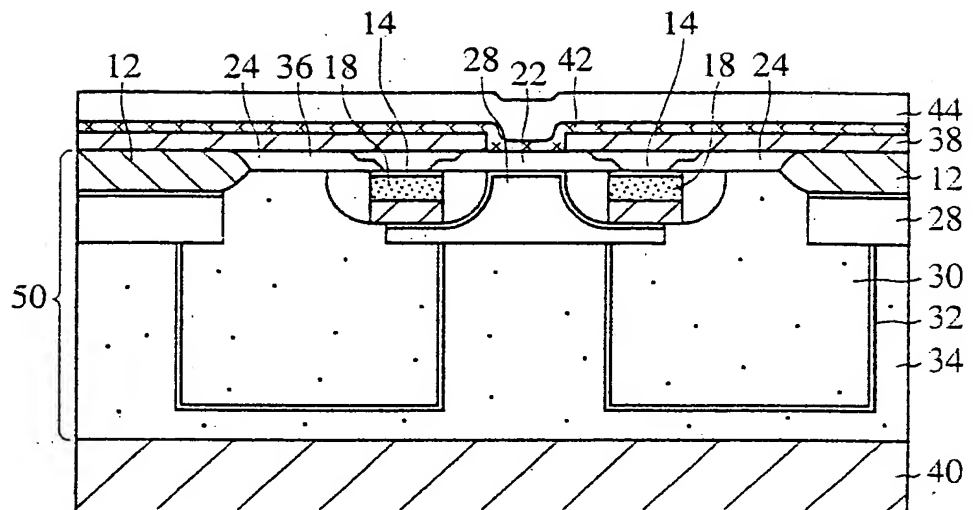
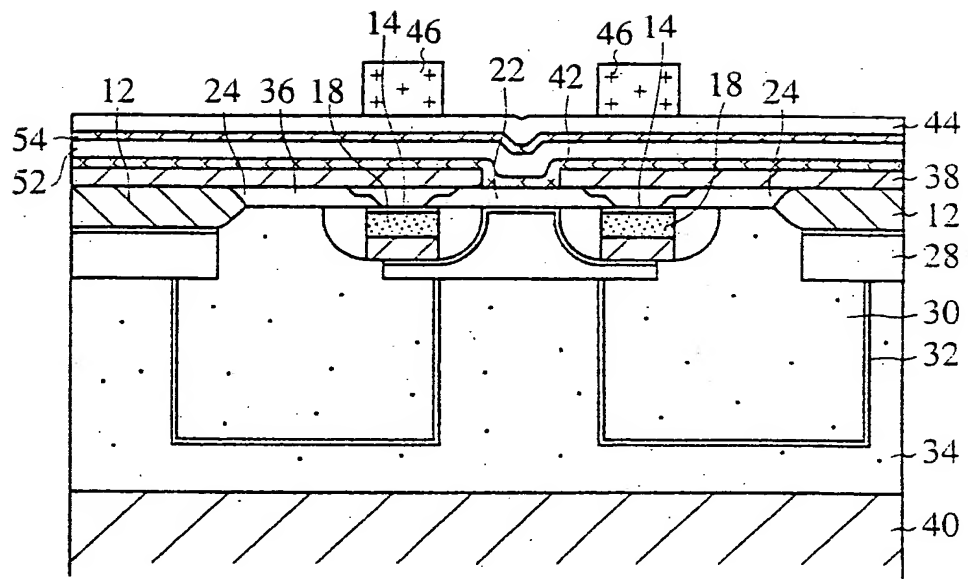
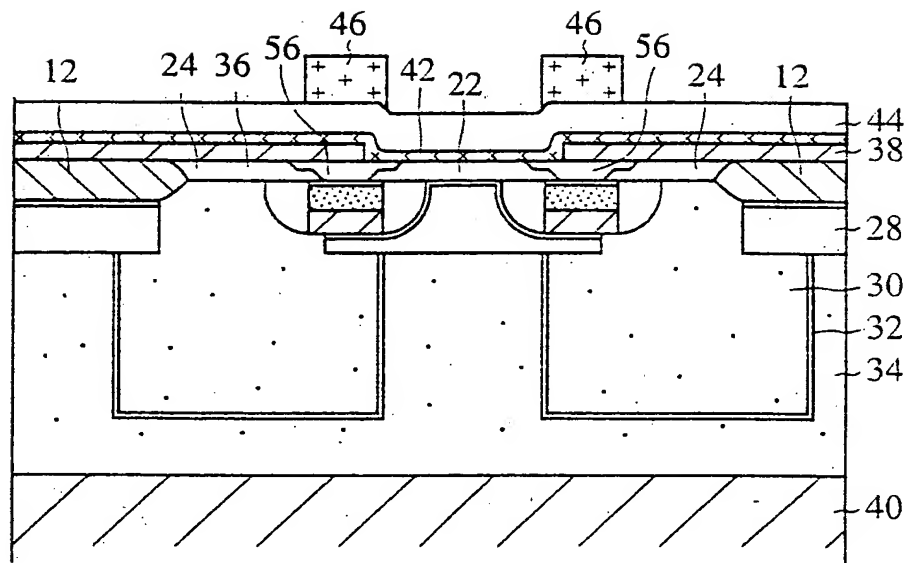


FIG.7



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FIG.8



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FIG.9

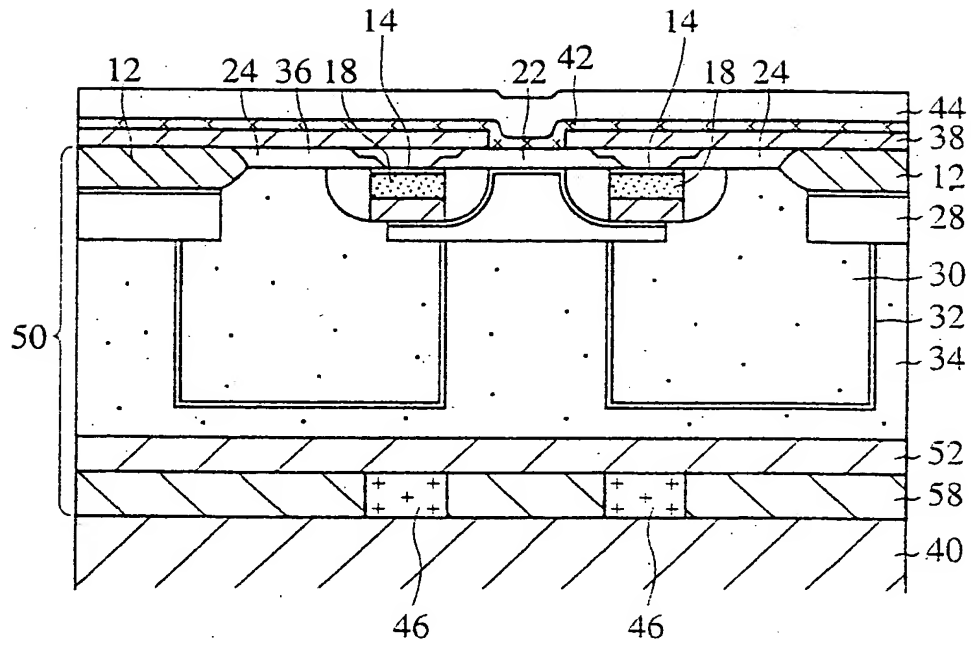


FIG.10A

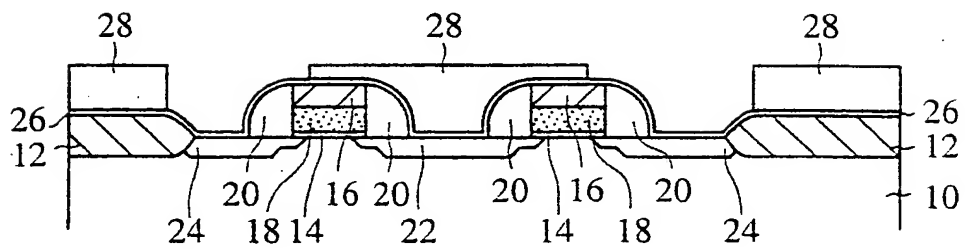


FIG.10B

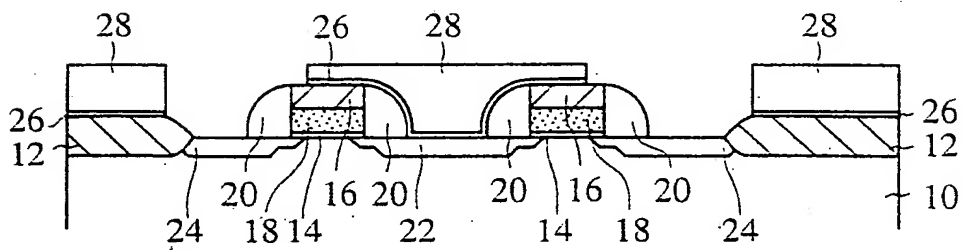
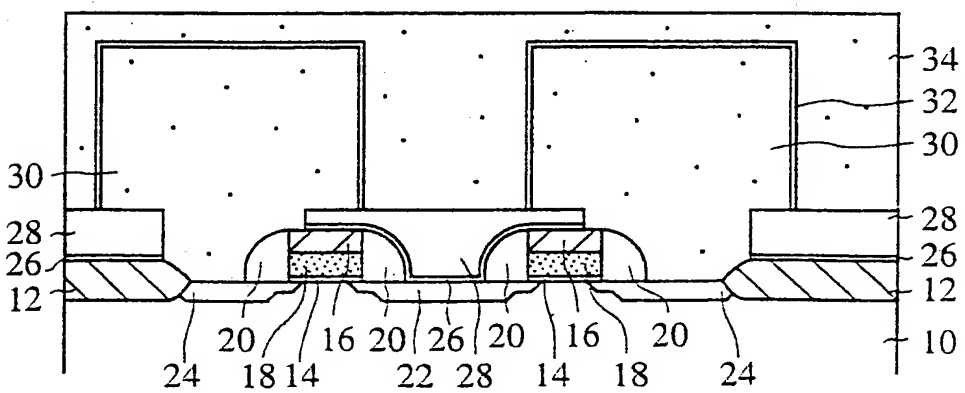


FIG.10C



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FIG.11A

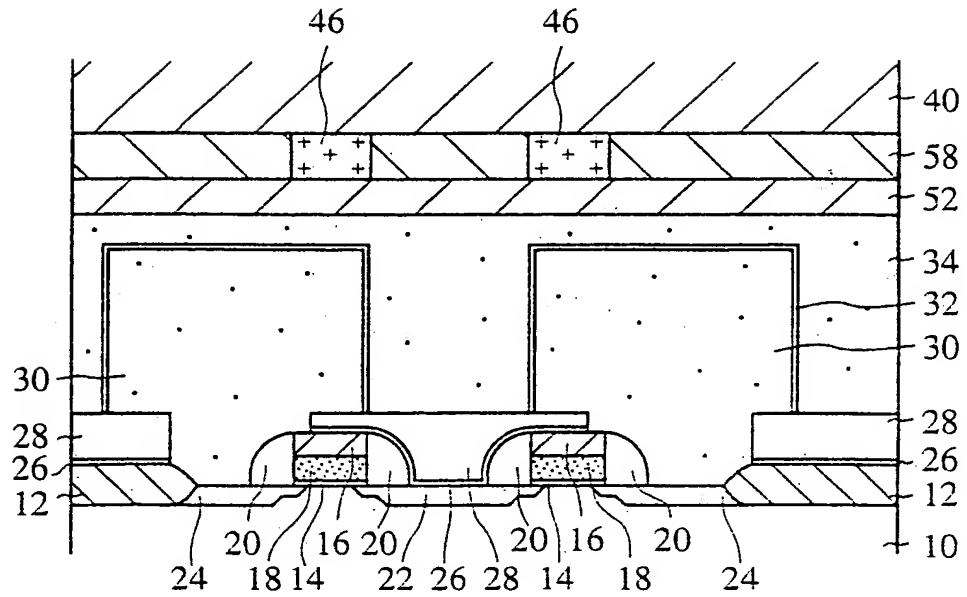


FIG.11B

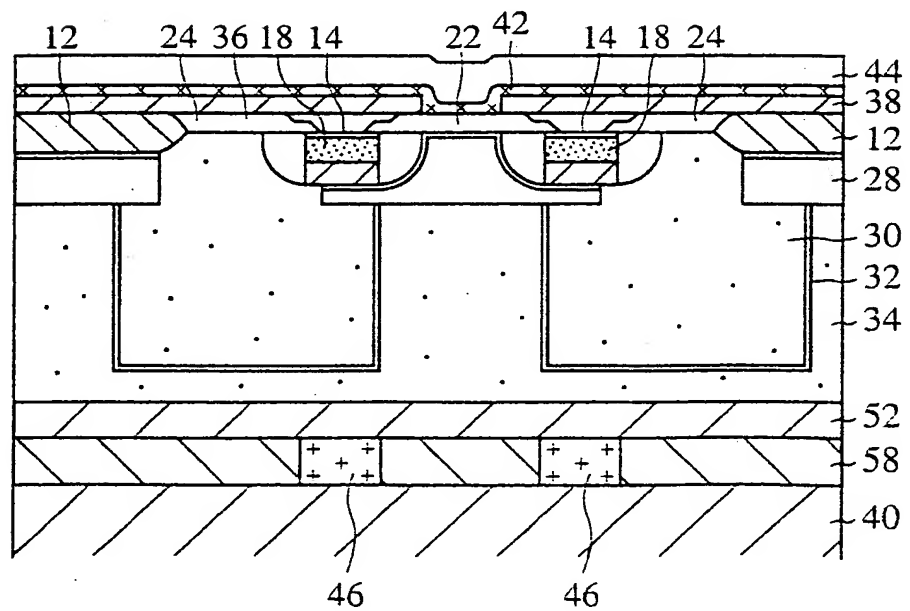


FIG.12A

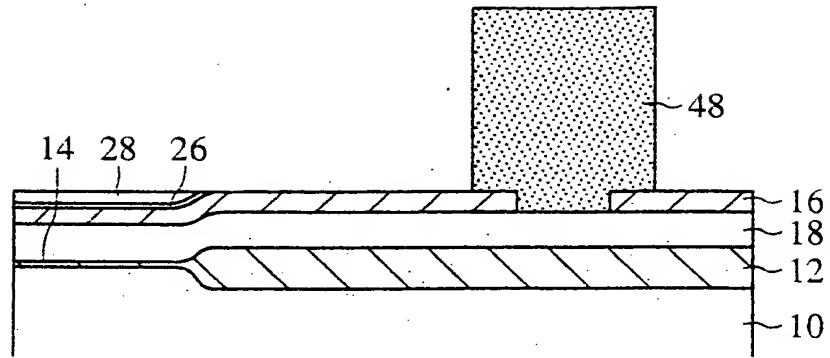


FIG.12B

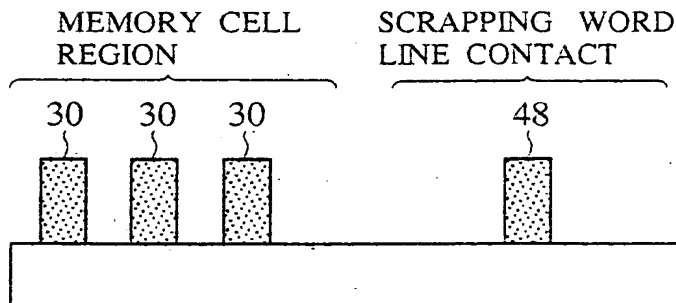


FIG.12C

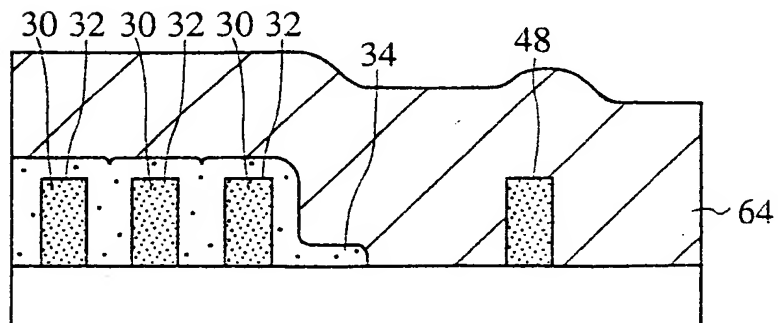


FIG.13A

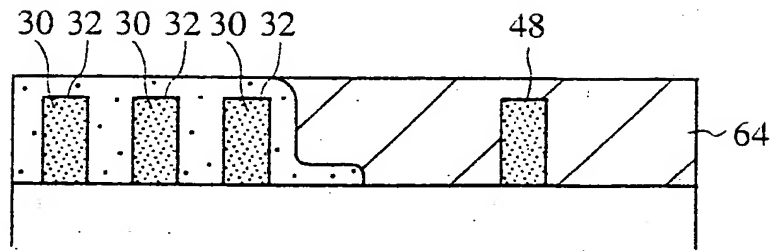


FIG.13B

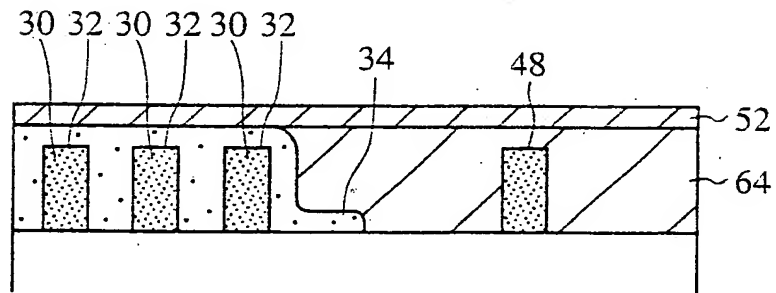


FIG.13C

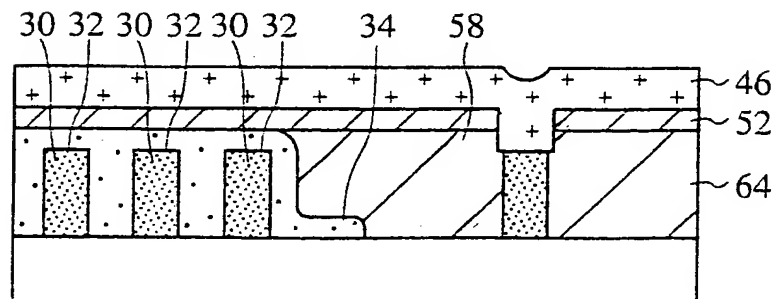


FIG. 14

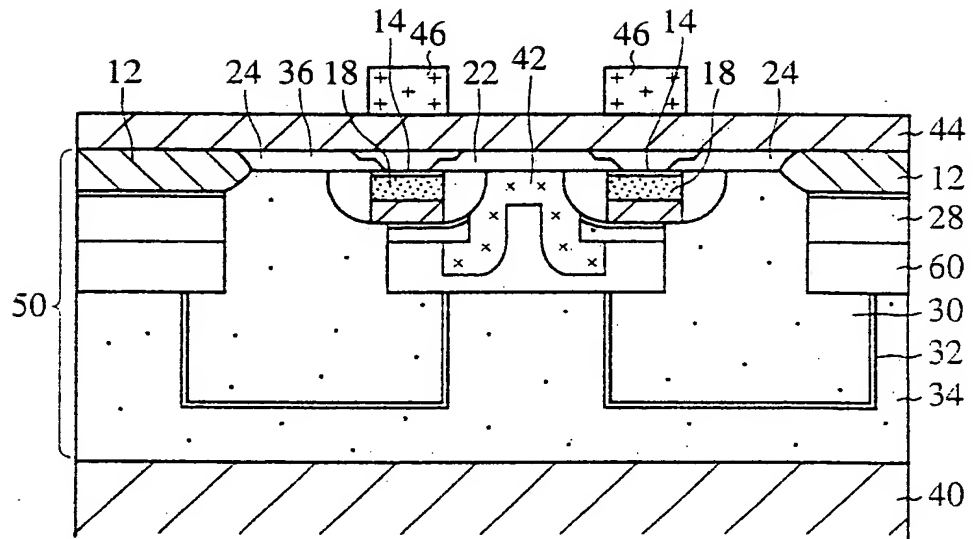


FIG.15A

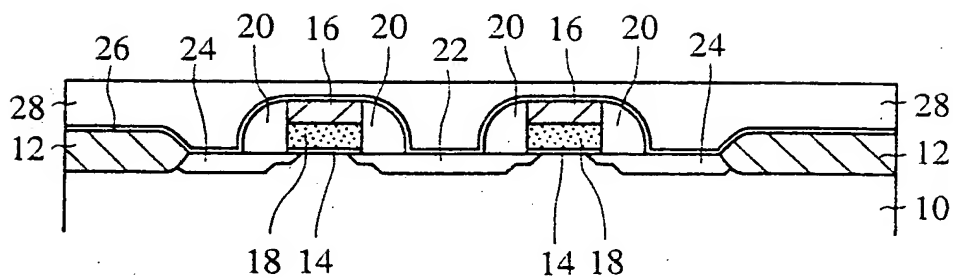


FIG.15B

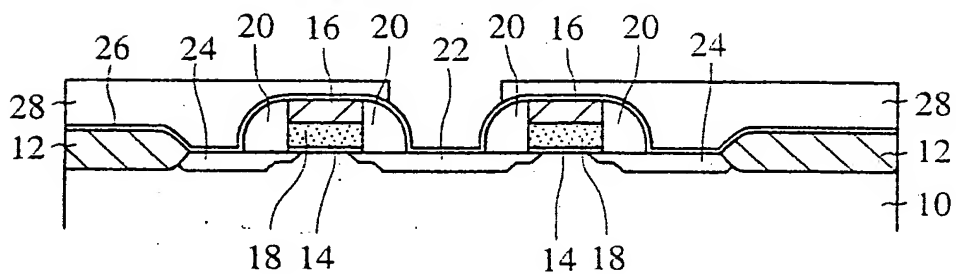
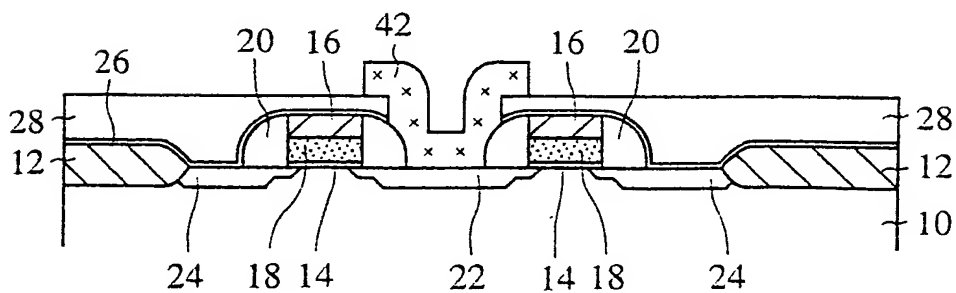


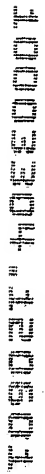
FIG.15C



[illegible]

This diagram shows a cross-sectional view of a semiconductor device. A central gate structure (22) is positioned over a channel region (20). The gate structure includes a gate dielectric (42) and a gate electrode (28). The channel region (20) is formed in a substrate (10) and is surrounded by a gate dielectric (12). The device also features side gates (14, 18) and a source/drain region (24). The diagram includes a vertical scale on the right with values 10, 12, 28, 60, 30, 32, 34, and 40.

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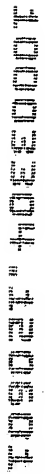


FIG.18A

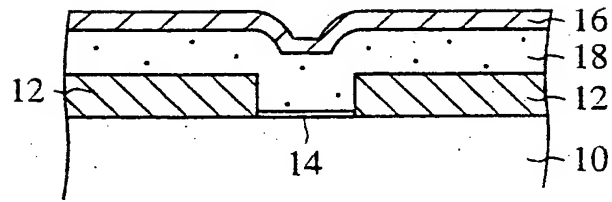
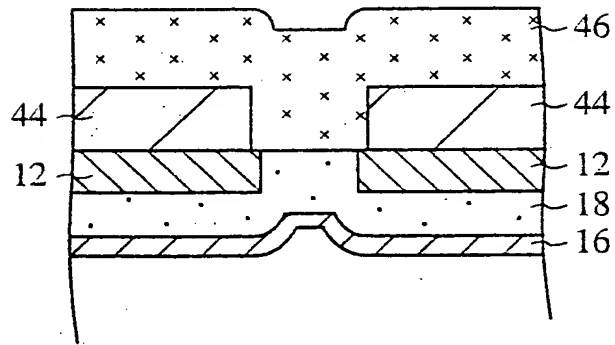
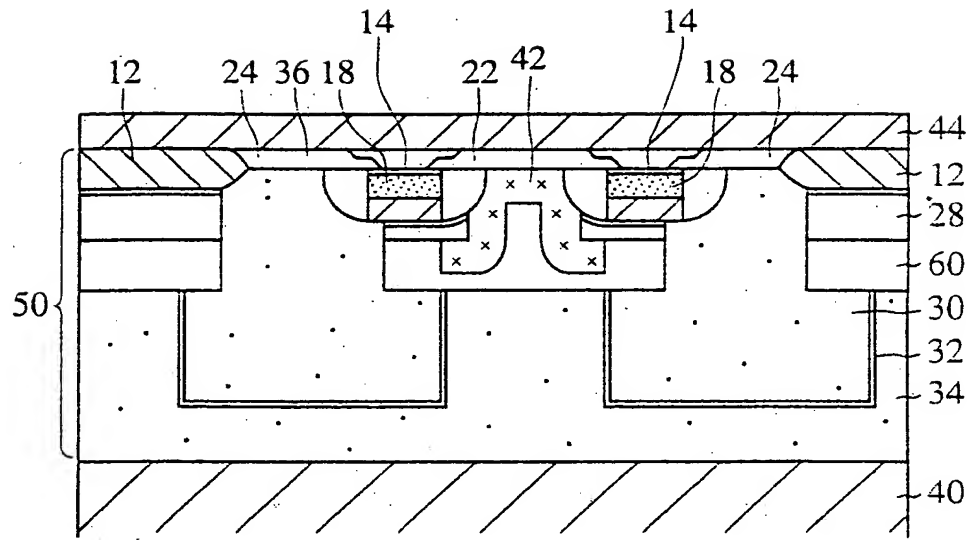


FIG.18B



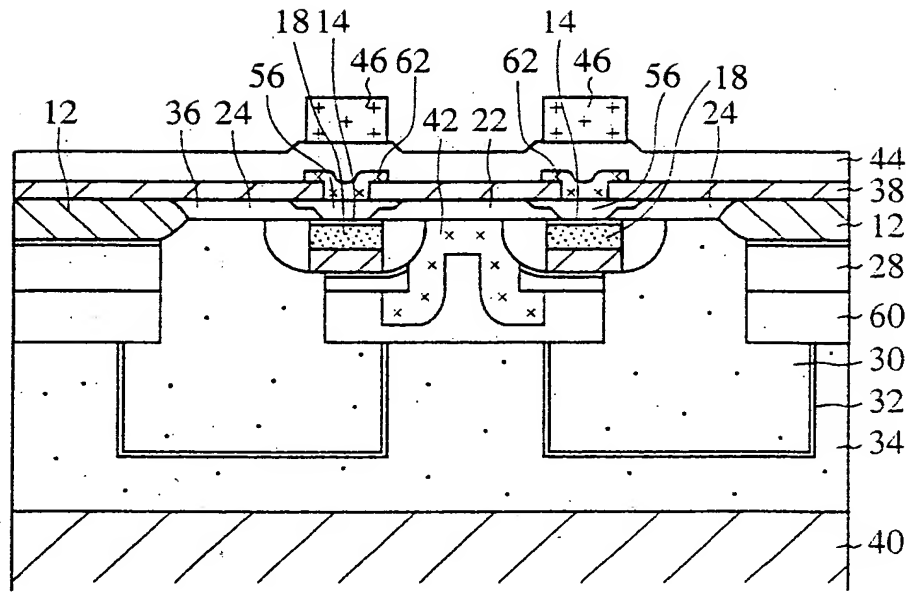
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FIG.19



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FIG.20



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FIG.22A

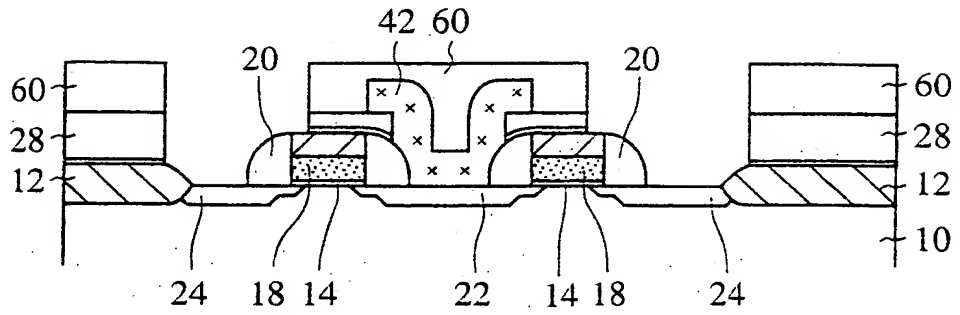


FIG.22B

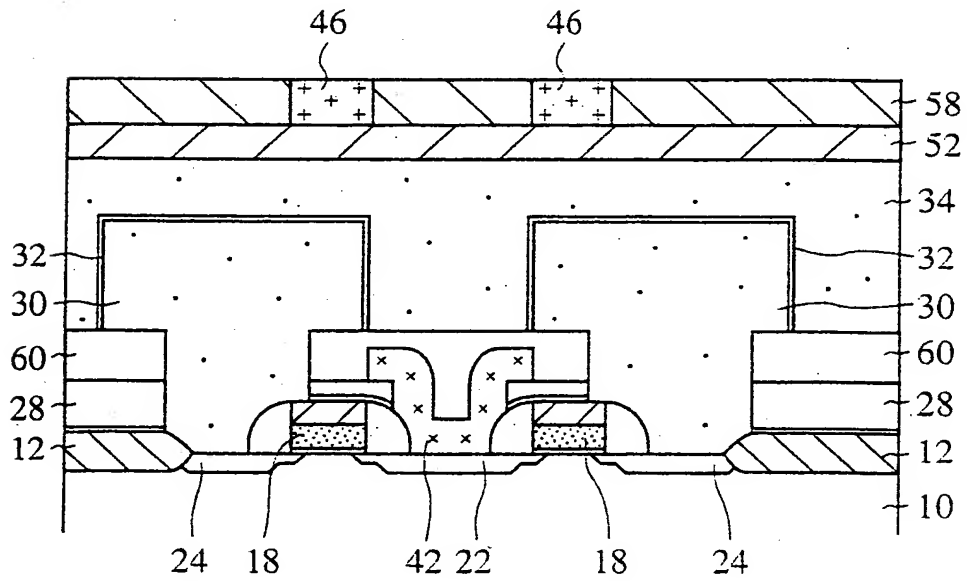


FIG. 22A

FIG.23A

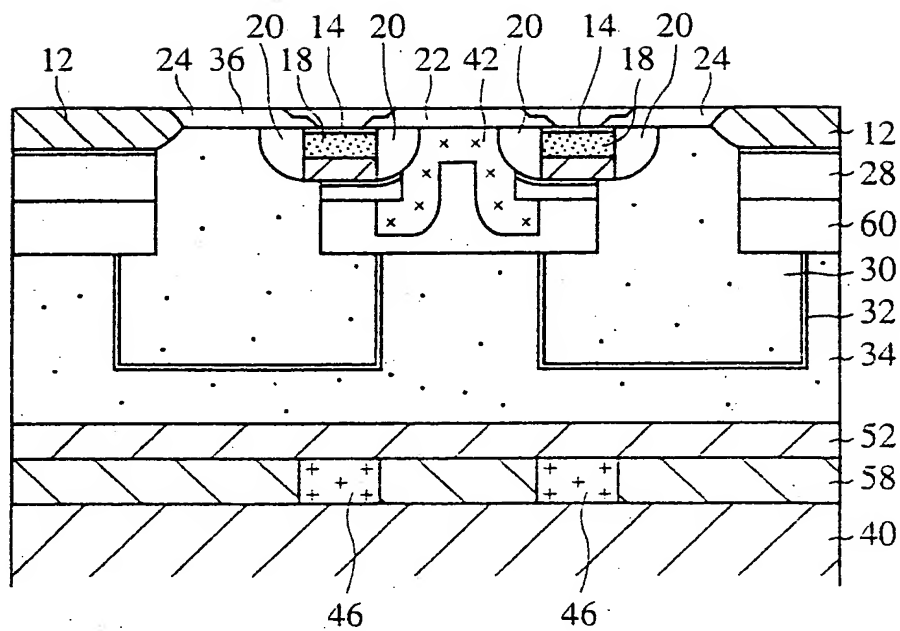


FIG.23B

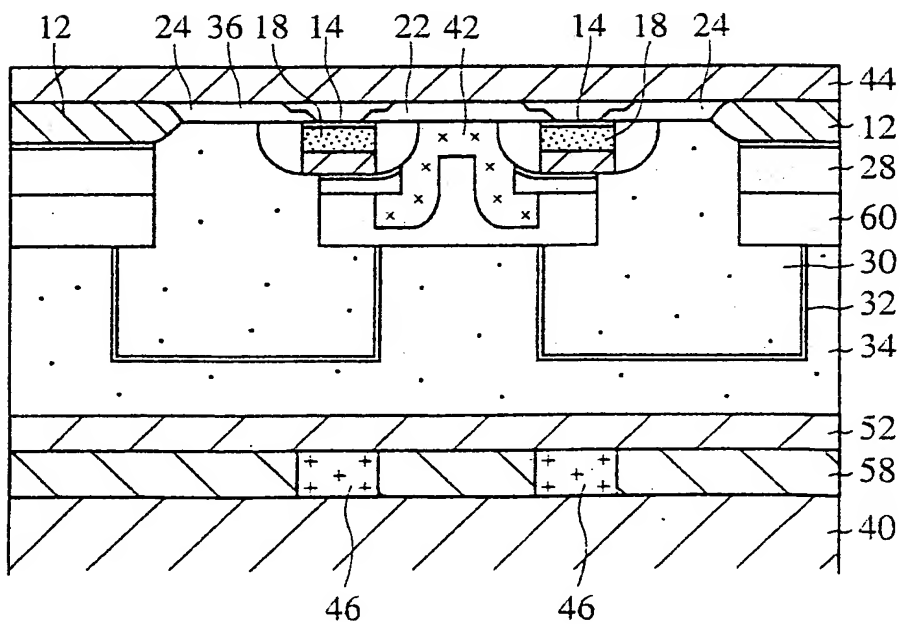


FIG.24

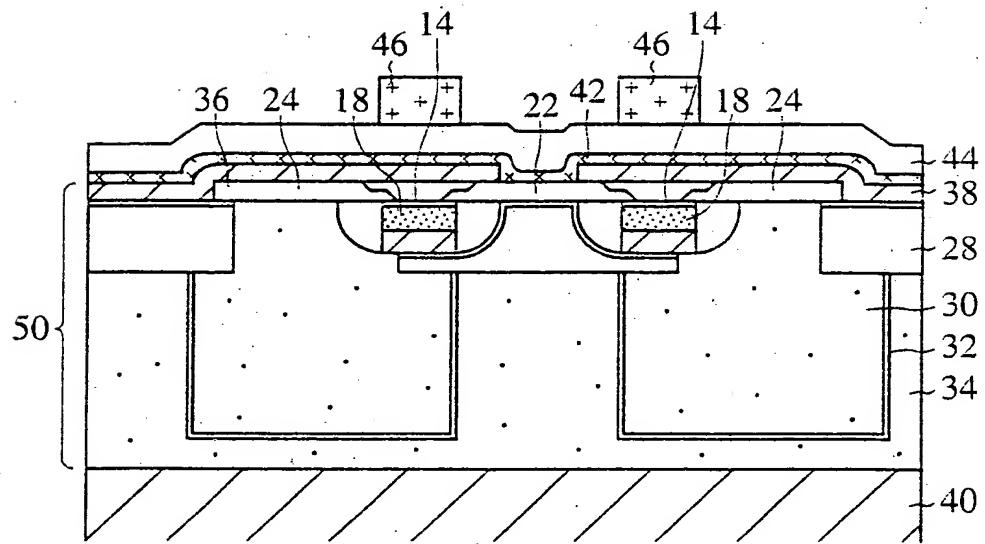


FIG. 24

FIG.25A

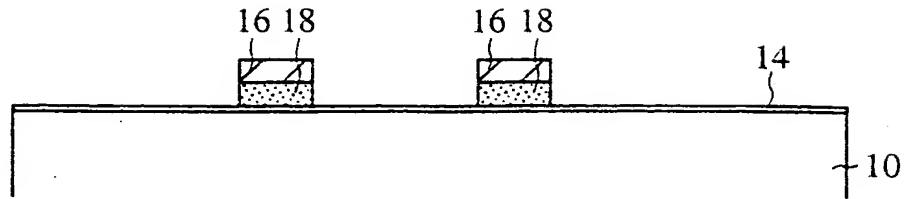


FIG.25B

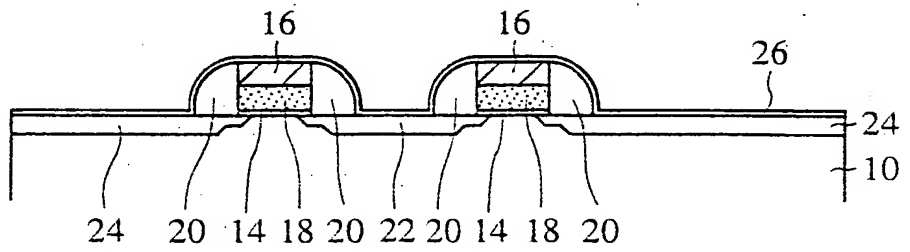


FIG.25C

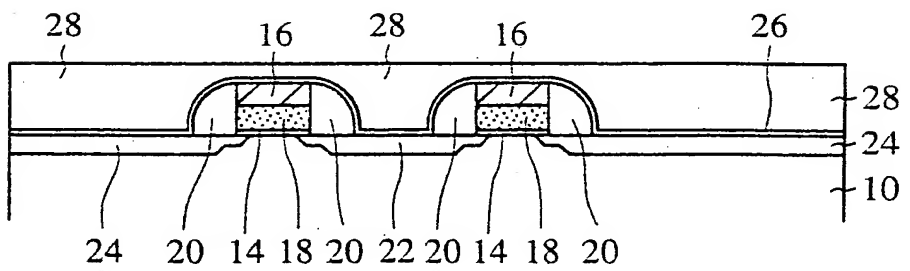


FIG.25D

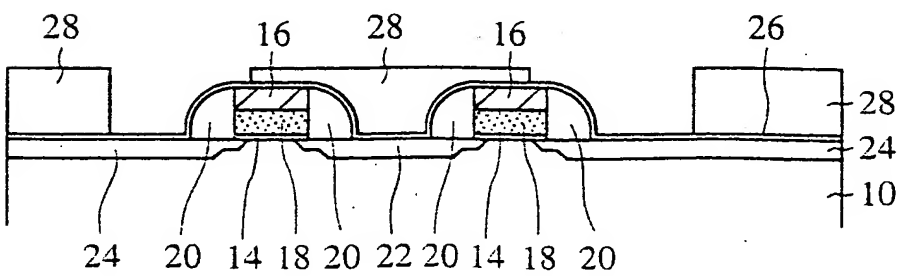


FIG.26A

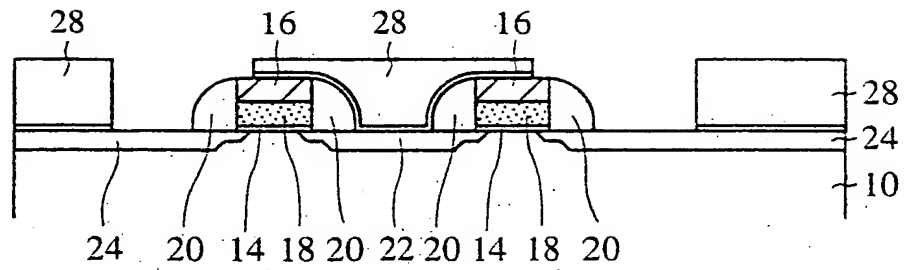
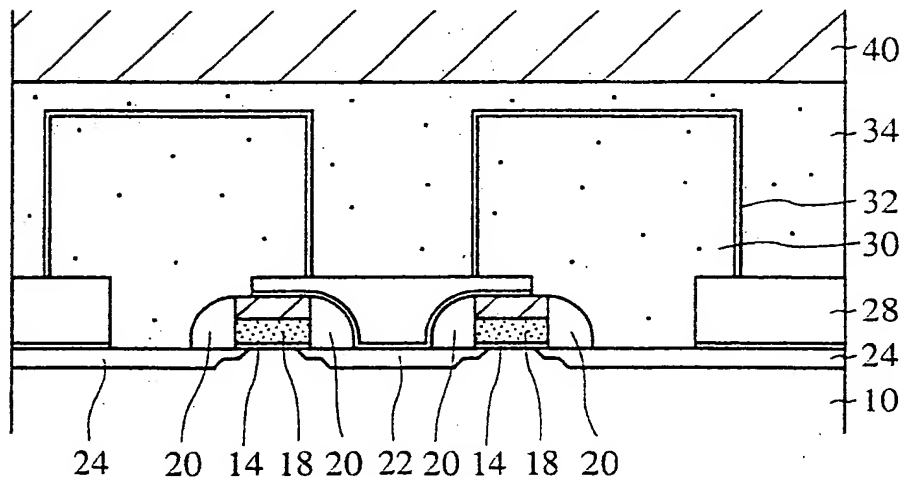


FIG.26B



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FIG.27A

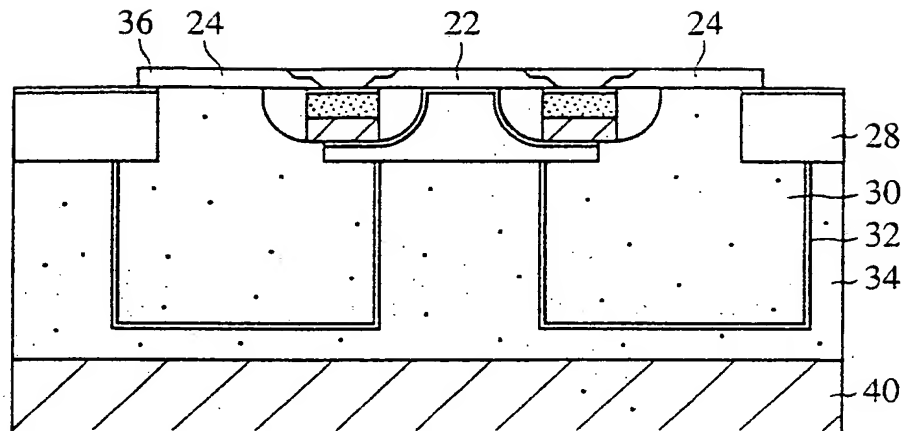


FIG.27B

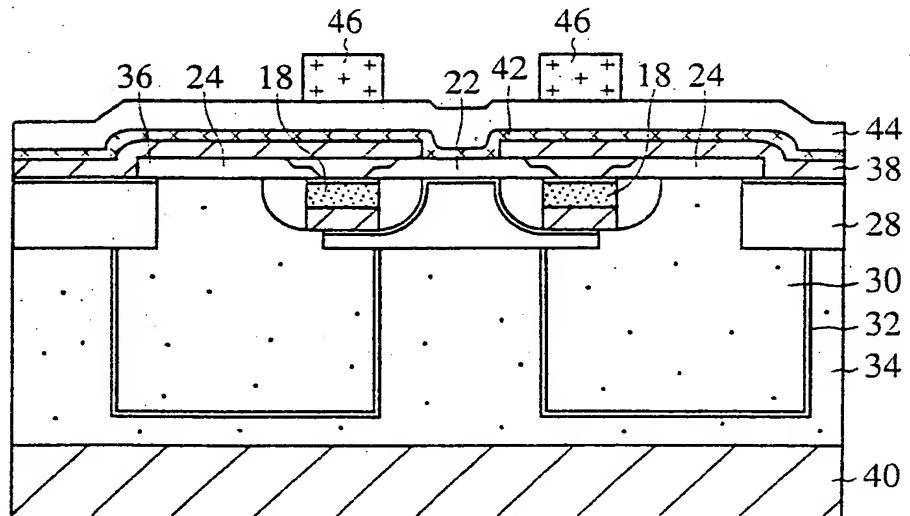
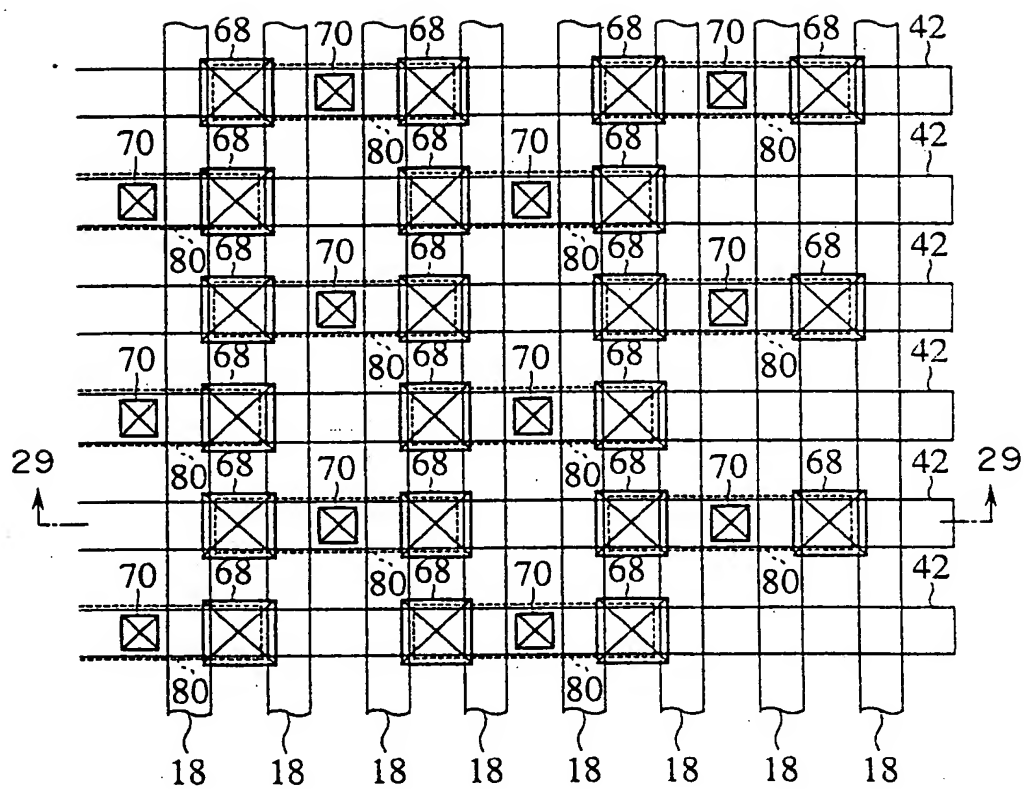


FIG.28



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FIG. 29

FIG. 29

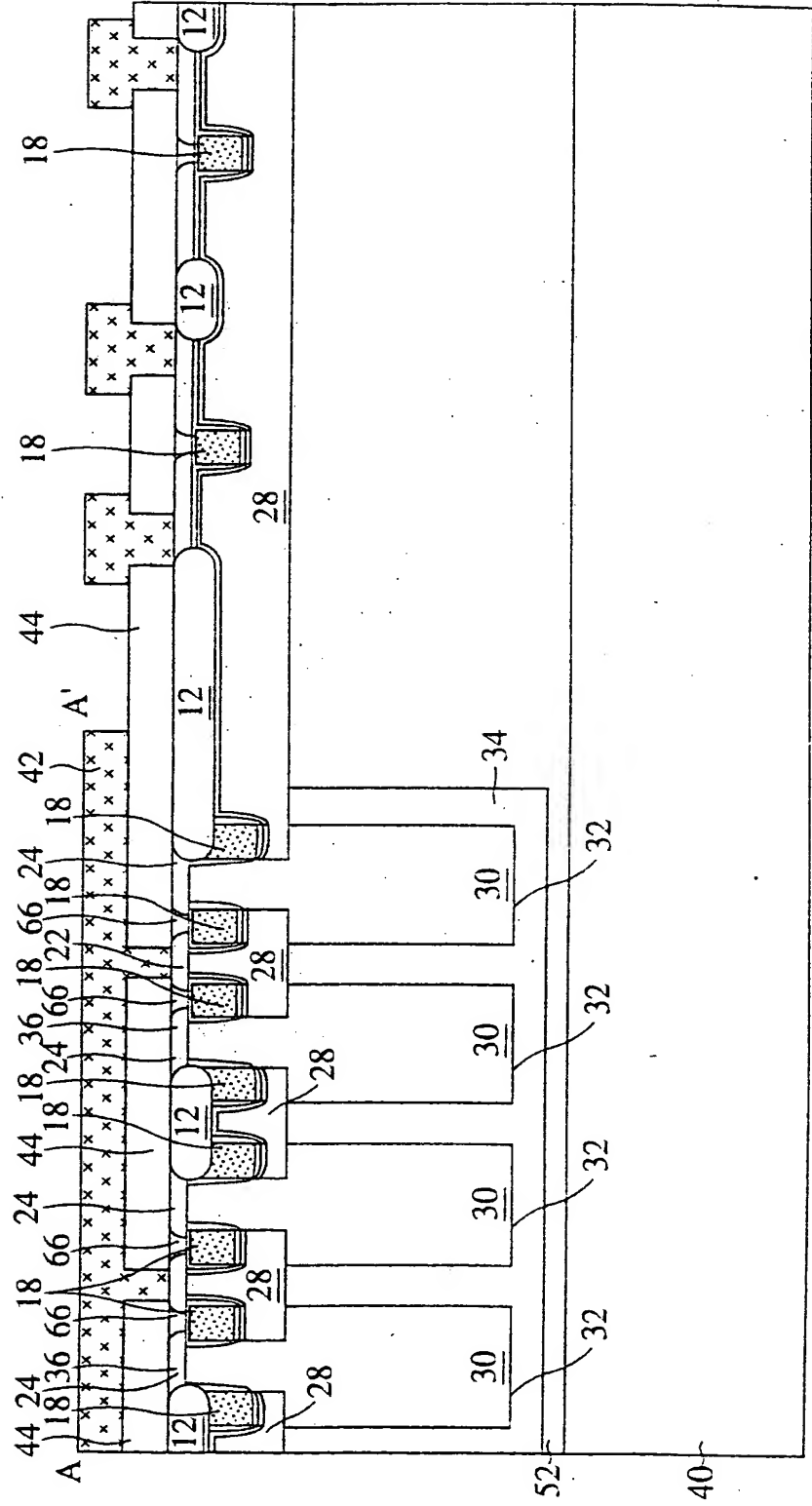
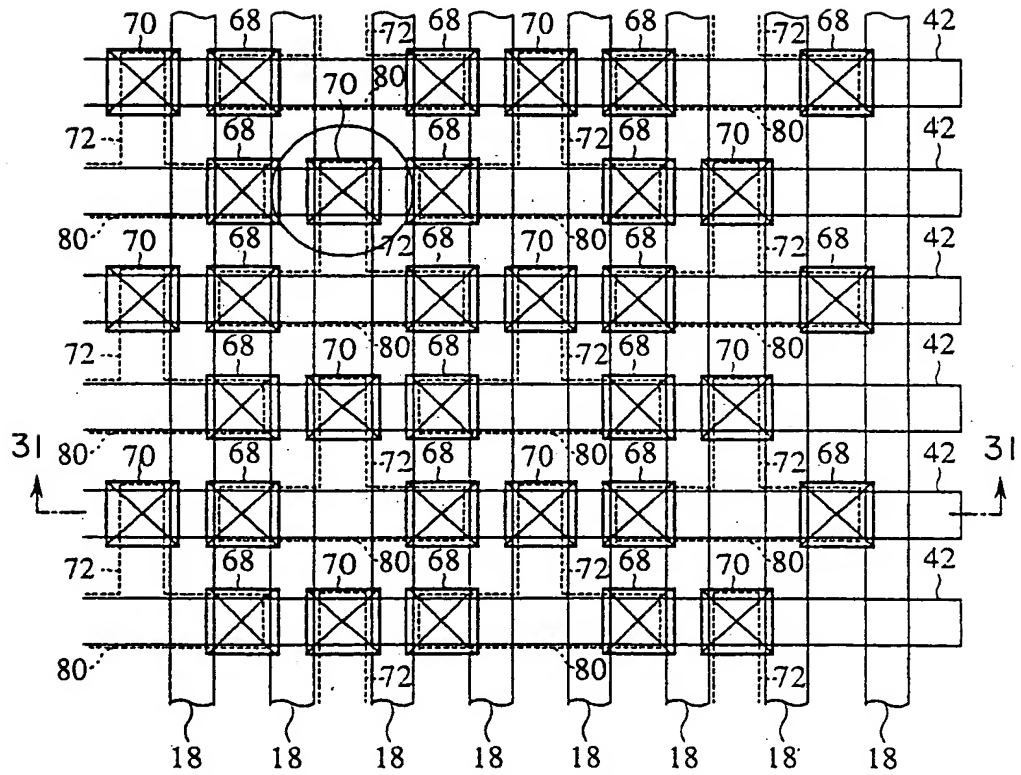


FIG.30



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FIG.31

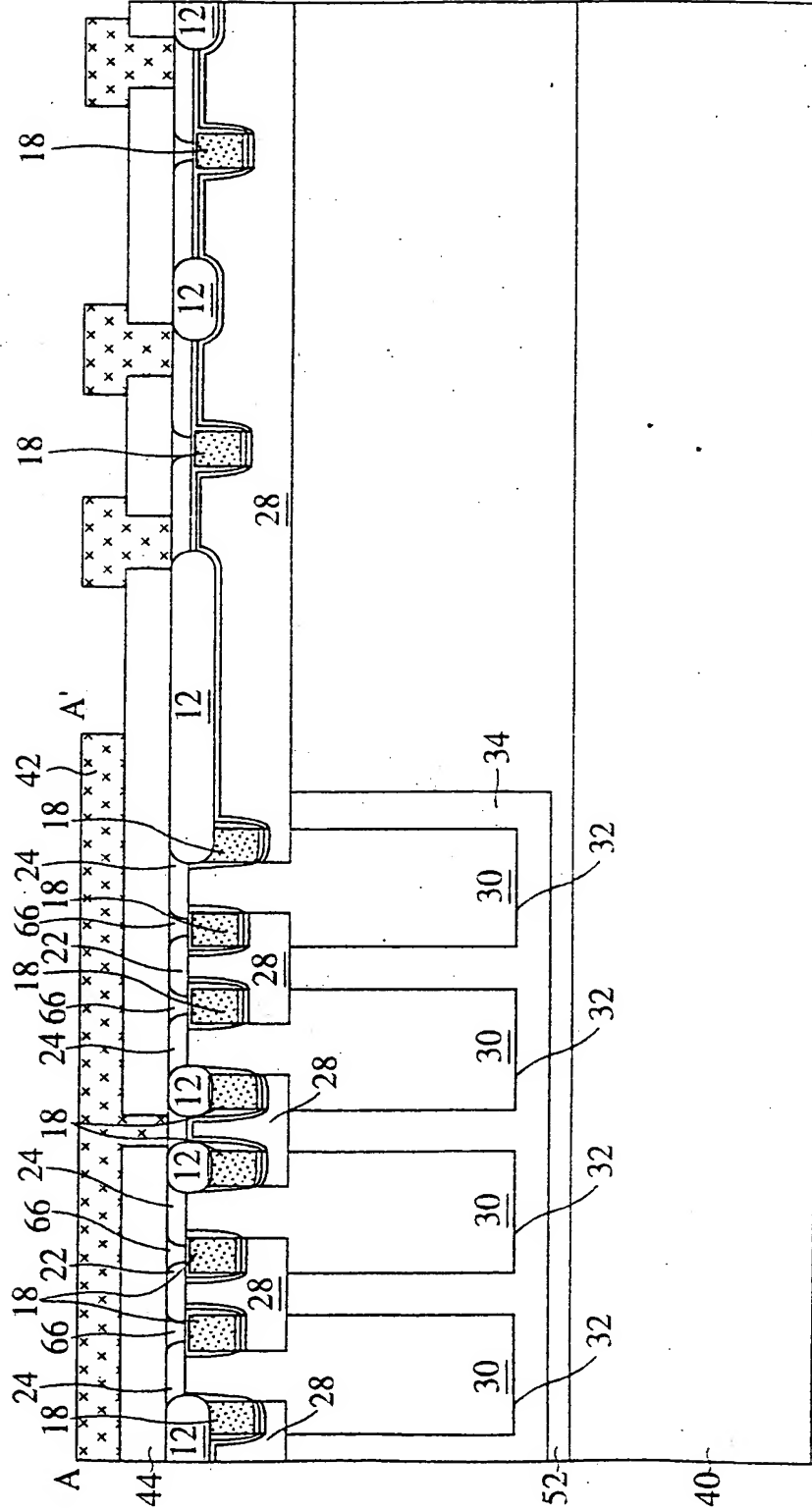


FIG.32

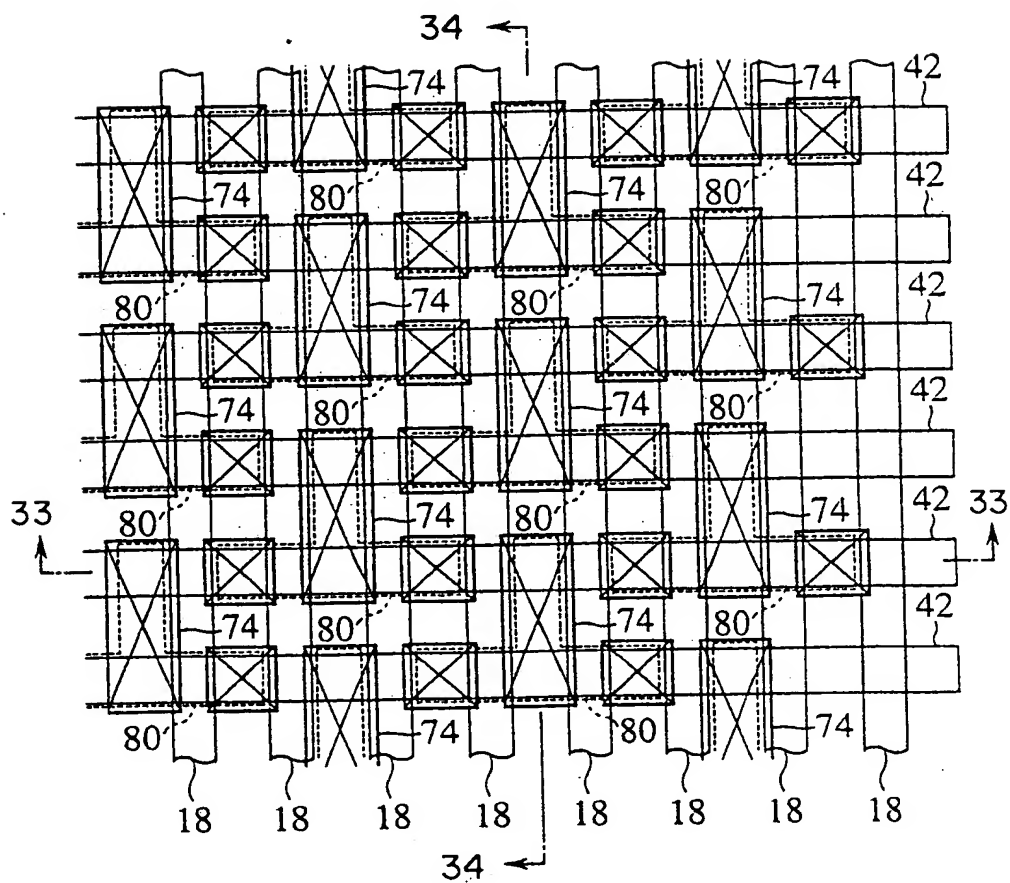
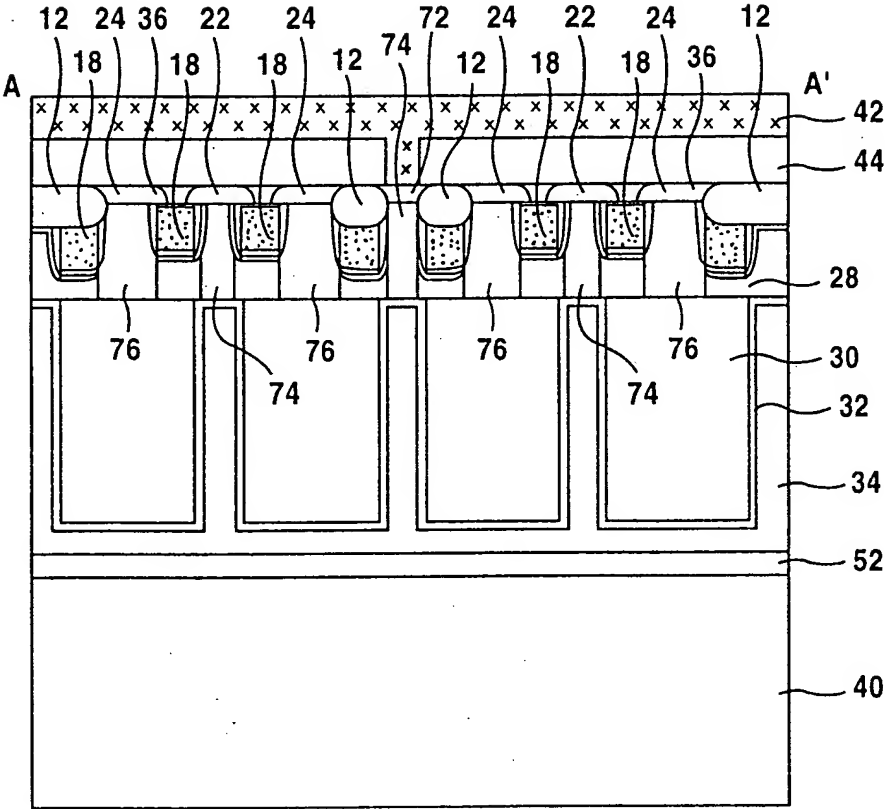
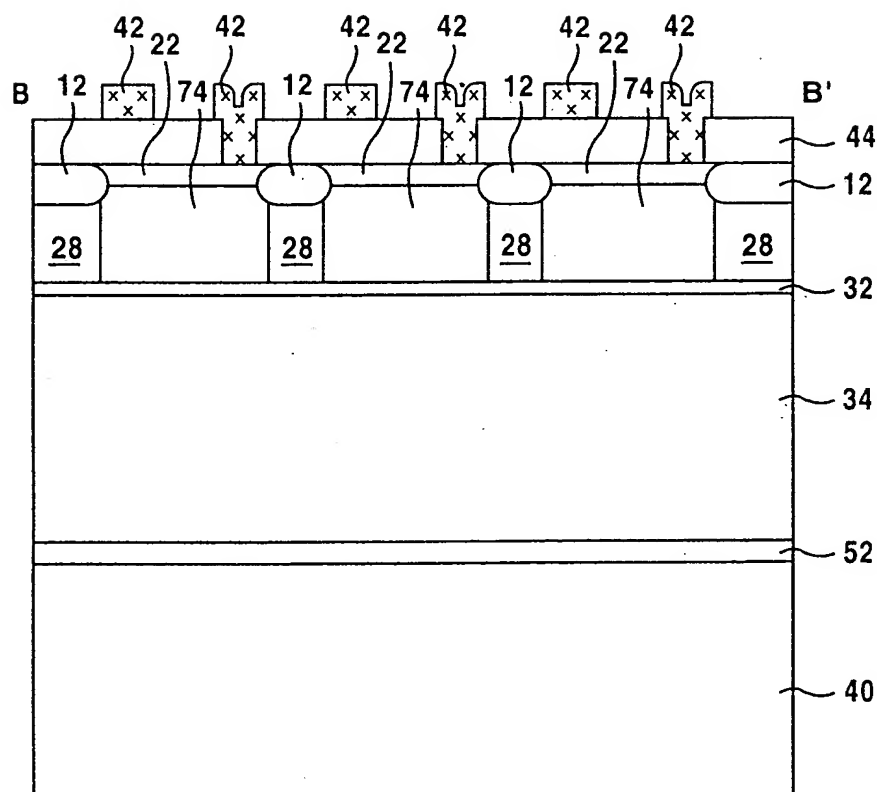


FIG.33



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FIG.34



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FIG. 35B

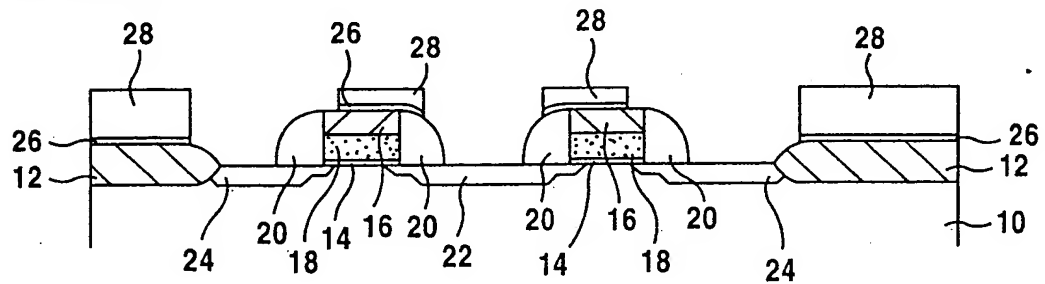


FIG. 35D

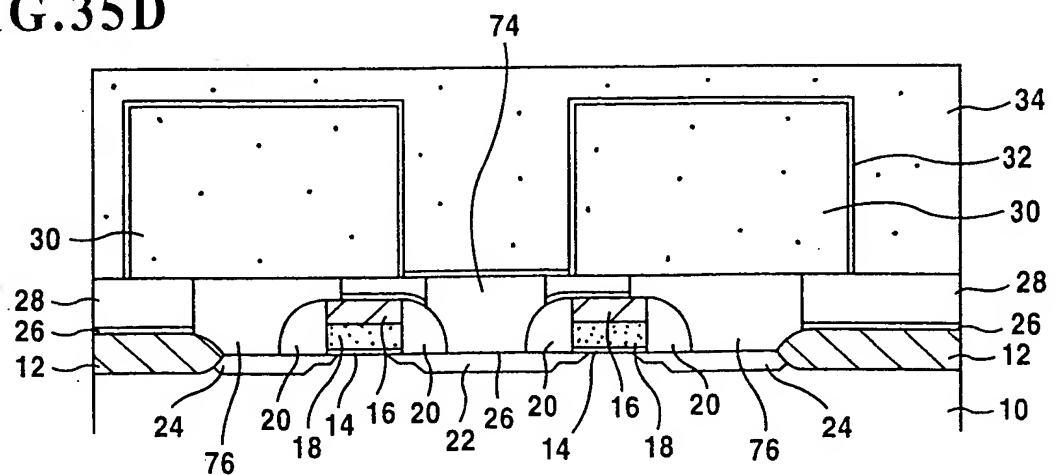


FIG.35E

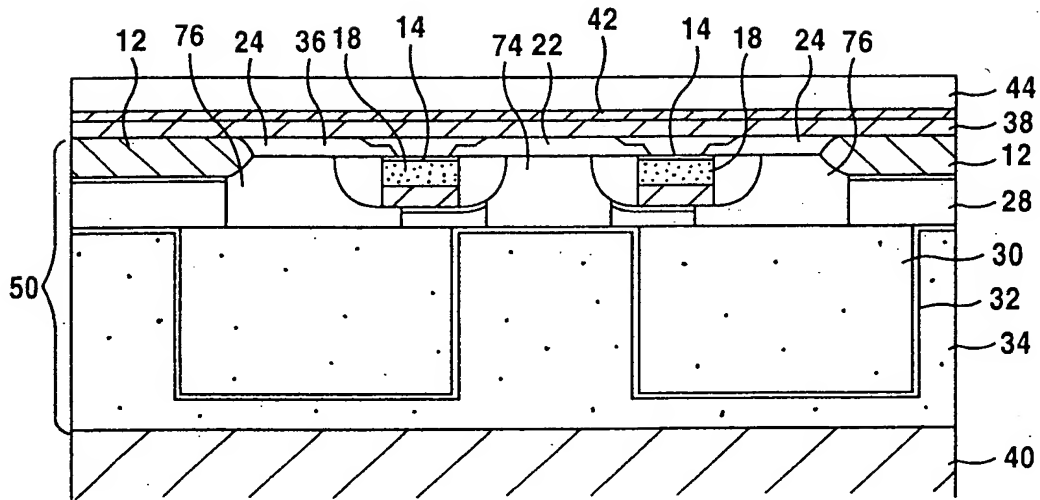


FIG.36

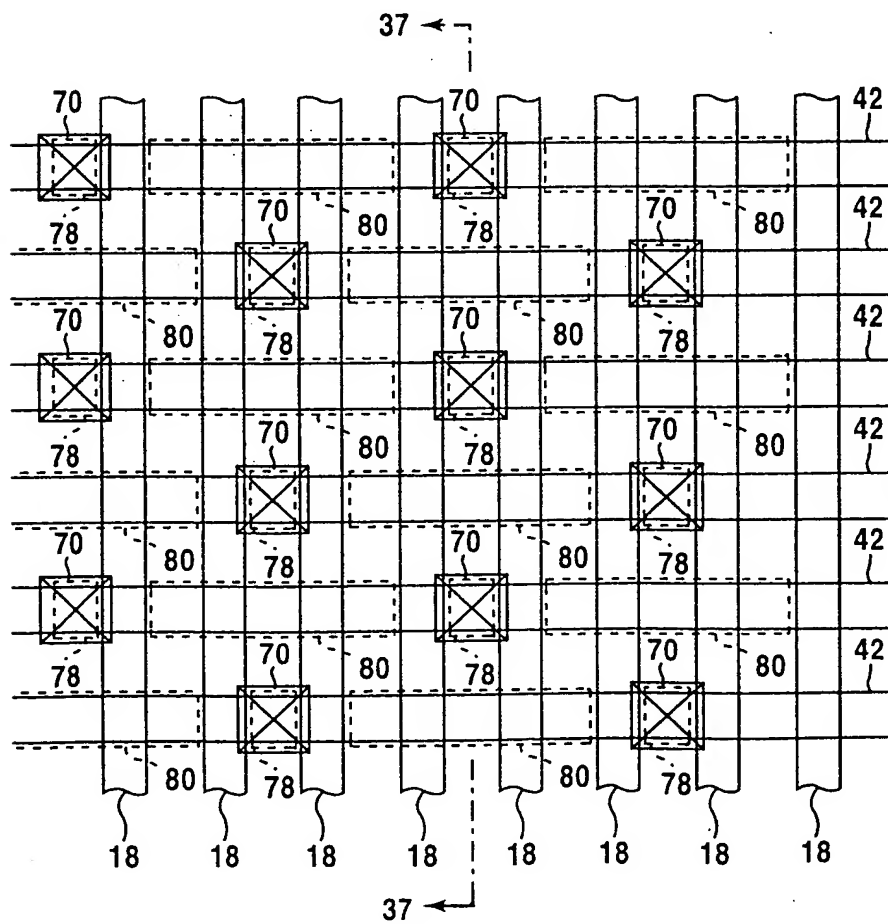
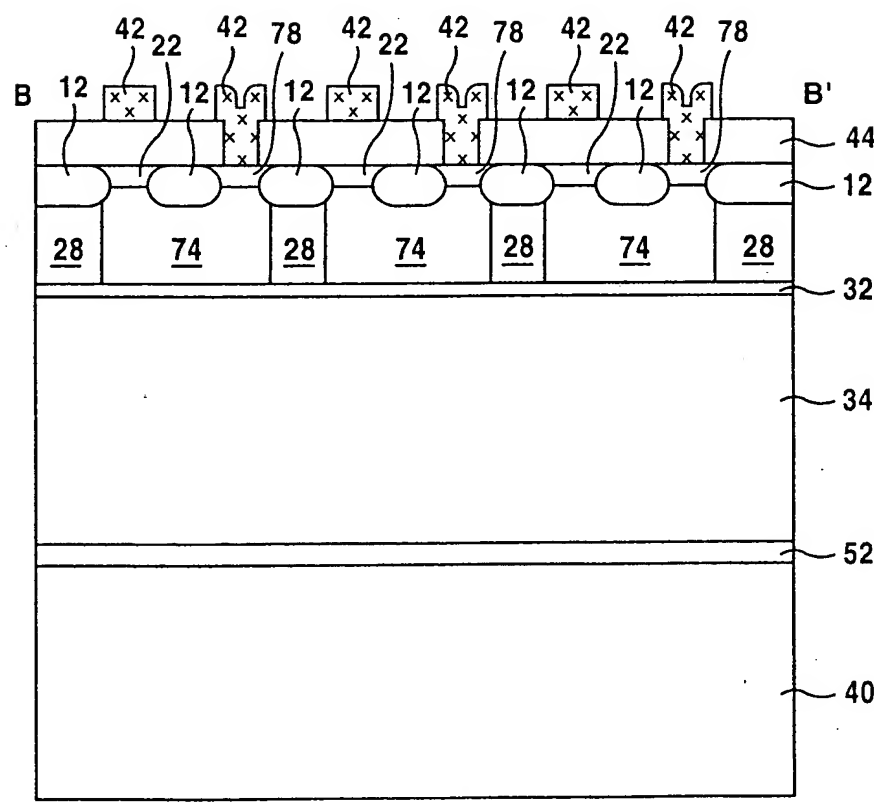


FIG.37



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FIG.38

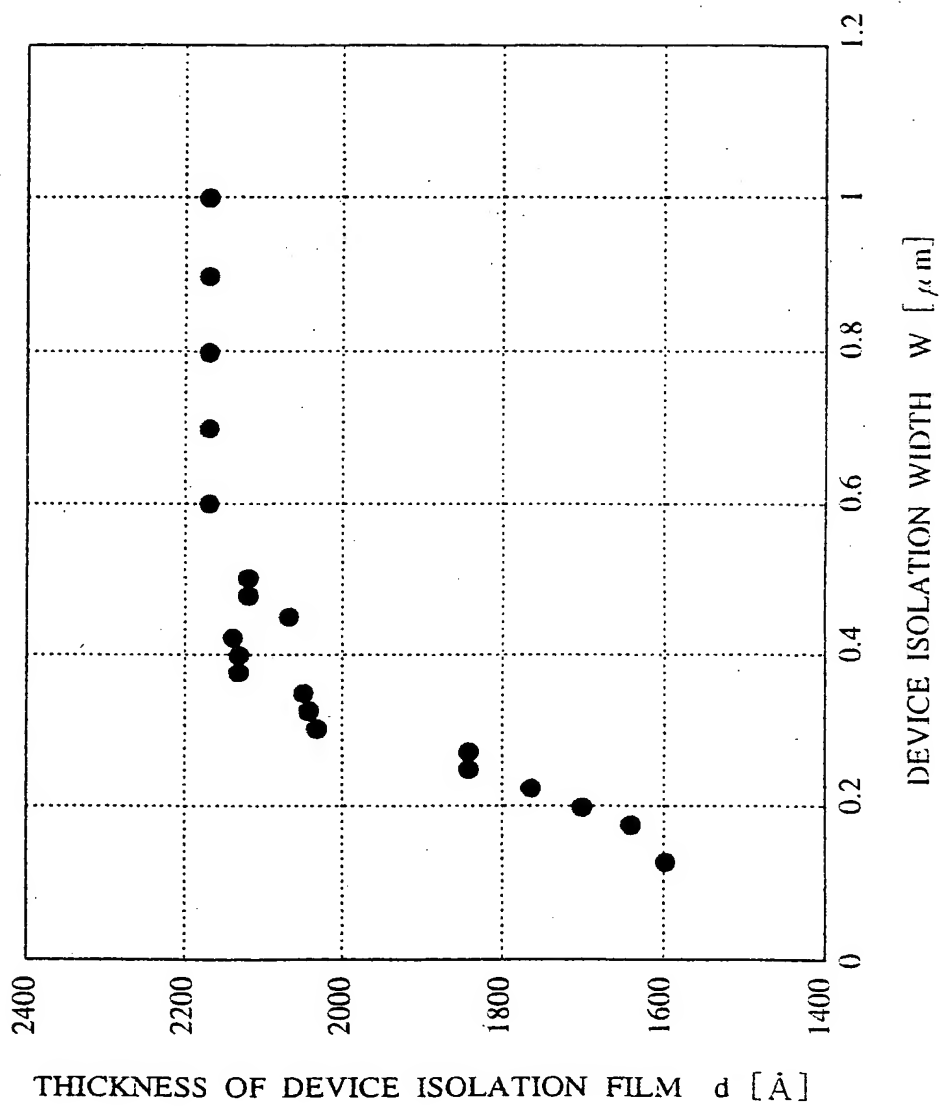


FIG.39A

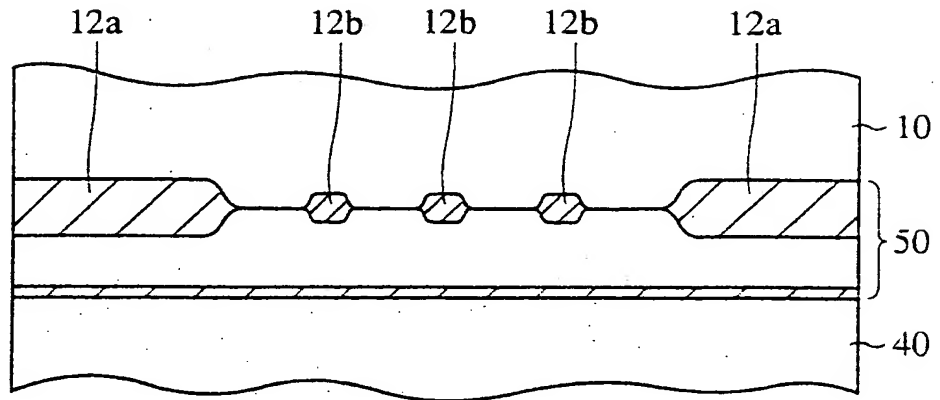


FIG.39B

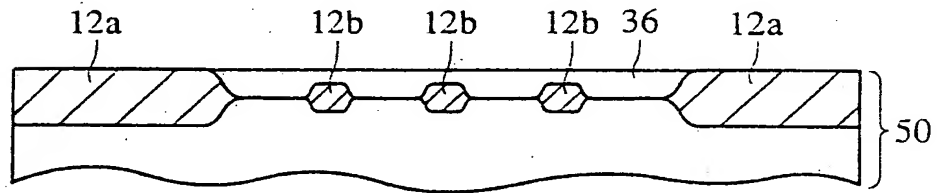


FIG.39C

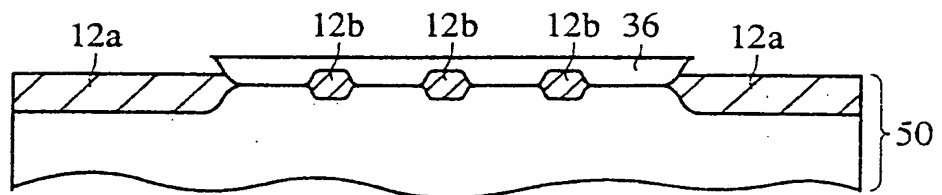


FIG.39D

